FIG. 1 conceptually illustrates a dual mode BIST controller constructed and operated in accordance with the present invention in a block diagram of an application specific integrated circuit ("ASIC");

FIG. 2 depicts one particular embodiment of the LBIST domain of the dual mode BIST controller in **FIG. 1** in a block diagram;

FIG. 3 illustrates one particular embodiment of a state machine for the LBIST engine in the LBIST domain of **FIG. 2**;

FIG. 4 illustrates one particular embodiment of a multiple input signature register ("MISR") of the LBIST domain of **FIG. 2**, the contents of which is the LBIST signature;

FIG. 5 illustrates one particular embodiment of a register used in a pattern generator for the LBIST engine in the LBIST domain of **FIG. 2**;

FIG. 6 illustrates one particular embodiment of the MBIST domain of the of the dual mode BIST controller in **FIG. 1** in a block diagram;

FIG. 7 illustrates one particular embodiment of a MBIST signature register of the MBIST domain of **FIG. 2**, the contents of which is the MBIST signature in accordance with one aspect of the present invention;

FIG. 8 illustrates one particular embodiment of a state machine for an MBIST engine in the MBIST domain of **FIG. 2**; and

FIG. 9 illustrates the LBIST engine of **FIG. 1** and **FIG. 2** providing clock signals to other parts of the ASIC in **FIG. 1** in one particular embodiment of the invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous

implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort, even if complex and time-consuming, would be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

FIG. 1 conceptually illustrates a dual mode **b**uilt-**i**n **s**elf-**t**est ("BIST") controller 100 constructed and operated in accordance with the present invention. In the illustrated embodiment, the controller 100 comprises a **l**ogic **BIST** ("LBIST") engine 110, a **m**emory **BIST** ("MBIST") engine 120, a LBIST signature 130, and a MBIST signature 140 separated into a LBIST domain 160 and a MBIST domain 170. Note that some embodiments may omit the MBIST signature 140 in accordance with conventional practice. The LBIST signature 130 and the MBIST signature 140 are the contents of memory elements of the BIST controller 100, such as registers, as is discussed further below.

The controller 100 comprises a portion of an integrated circuit device, *i.e.*, an **a**pplication **s**pecific **i**ntegrated **c**ircuit ("ASIC") 150. The ASIC 150 includes a testing interface 180, preferably a **J**oint **A**ction **T**est **G**roup ("JTAG") tap controller, through which the BIST of the dual mode BIST controller 100 can be invoked and through which the results may be returned in accordance with conventional practice. The ASIC 150 also includes one or more memory components 190, preferably **s**ynchronous **r**andom **a**ccess **m**emories ("SRAMs"), and combinatorial logic in a plurality of timing domains 195a-d that are tested by the BIST of the dual mode BIST controller 100.

The dual mode BIST controller 100 includes three frequency domains—one in the LBIST domain 160, one in the MBIST domain 170, and a third in which the signals from the testing interface 180 operate. In one particular embodiment, the LBIST domain 160 operates on a 10 MHz clock signal, the MBIST domain 170 operates on a 75 MHz clock signal, and the third domain operates at a 10 MHz clock signal in accordance with the JTAG standard. In this particular embodiment, the 75 MHz clock signal is obtained by splitting the 150 MHz clock signal, as will be discussed further below, and the 10 MHz LBIST clock signal is generated based on the 10 MHz JTAG clock signal.

In accordance with the present invention, the LBIST clock signal (not shown) operates at the lowest frequency of any of the logic involved in the LBIST. This includes the combinatorial logic under test, *e.g.*, the combinatorial logic in the timing domains 195a-d, or in the control logic, *i.e.*, the testing interface 180. Typically, the combinatorial logic of the ASIC core operates on several different frequencies defining different timing domains such as the timing domains 195a-d. These frequencies may be different from those employed by the control logic. Consider, for instance, an embodiment where the testing interface 180 operates at 10 MHz in accordance with the JTAG standard; the timing domain 195a operates at 150 MHz; and, the timing domains 195b-d operate at a variety of frequencies ranging from 66MHz to 133 MHz. The LBIST performed by the LBIST engine 110 will, in this particular implementation, be performed in all timing domains 195a-d at 10 MHz, which is the slowest frequency, to avoid timing errors. Thus, the present invention employs a slow LBIST to preserve timing integrity across all the timing domains while reducing the number of LBIST engines 110 needed to perform the LBIST on any given ASIC.

Because the dual mode BIST controller 100 can perform both the LBIST and the MBIST, all BIST functionality can be centralized in one location. Thus, the BIST functionality of the ASIC 150 can be designed in a single module. Note that the manner in which the clock signal for the MBIST domain 170 is implemented facilitates this feature. Furthermore, the BIST functionality can usually be designed in the geographic center of the ASIC 150. This feature facilitates the placement of other components, *e.g.*, the memory components 190, the logic in the timing domains 195a-d, and the routing of connections. As will be appreciated by those skilled in the art having the benefit of this disclosure, the memory components 190 are typically large relative to other components of the ASIC 150. Their placement therefore tends to dictate the location of other components, *e.g.*, the dual mode BIST controller 100, on the ASIC 150. Consequently, in some embodiments, the dual mode BIST controller 100 might not be located at the geographical center of the ASIC 150. However, most design techniques will result in the memory components being located at the corners of the ASIC 150, as shown in **FIG. 1**. The dual mode BIST controller 100 may therefore usually be geographically centralized.

One particular embodiment of the LBIST domain 160 is conceptually illustrated in **FIG. 2**. In this particular embodiment, the LBIST engine 110 comprises an LBIST state